In re Patent Application of
CAMBONIE
Serial No. **Not Yet Assigned**
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In the Claims:

Claims 1-10 (Cancelled).

11. (New) A configurable electronic circuit comprising:

at least one tile comprising a plurality of interconnected cells, each cell comprising

a multiplier,

an arithmetic and logic unit (ALU) for performing at least one arithmetic and/or logic function from a set of functions,

a vertical bus,

a first configurable switching circuit connected to said vertical bus and to inputs of said multiplier,

a second configurable switching circuit connected to said vertical bus and to an output of said multiplier,

a third configurable switching circuit connected to said vertical bus and to an output of said multiplier in a different cell,

a fourth configurable switching circuit connected to said vertical bus and to inputs of said ALU,

a fifth configurable switching circuit connected to said vertical bus and to an output of said ALU,

a carry propagation bus linking said ALU with said ALU in the different cell,

a configurable terminal switching circuit connected to said vertical bus, and

a horizontal bus linking said configurable terminal switching circuit with said configurable terminal switching circuit in the different cell.

12. (New) A configurable electronic circuit according to Claim 11, wherein said plurality of cells include first and second cells; wherein each multiplier comprises an m*n bit multiplier having two inputs for receiving two words of m and n bits respectively, and the output of each multiplier provides an output word of m+n bits; wherein said second configurable switching circuit in the first cell receives n bits of an output word delivered by said multiplier in the same cell; wherein said third configurable switching circuit of the first cell receives n bits of the output word delivered by said multiplier in the second cell; wherein said second configurable switching circuit in the second cell receives m bits of the output word delivered by said multiplier in the second cell; and wherein said third configurable switching circuit in the second cell receives m bits of the output word delivered by said multiplier in the first cell.

13. (New) A configurable electronic circuit according to Claim 12, wherein said vertical bus, said carry propagation bus and said horizontal bus each conveys words having a number of bits at least equal to a lowest common multiple of m and of n.

14. (New) A configurable electronic circuit according to Claim 12, wherein m is equal to n, and said vertical bus, said carry propagation bus and said horizontal

bus each comprises p tracks of n bits, with p being an integer greater than 1.

15. (New) A configurable electronic circuit according to Claim 11, wherein said at least one tile comprises a plurality of tiles interconnected.

16. (New) A configurable electronic circuit according to Claim 15, wherein said plurality of tiles are interconnected in a quincunx form.

17. (New) A configurable electronic circuit according to Claim 15, wherein said plurality of tiles include first and second tiles in a row; further comprising a sign extension module connected between said first and second tiles, said sign extension module being connected between said ALU in one cell in said first tile and said vertical bus of an immediately adjacent cell in said second tile.

18. (New) A configurable electronic circuit according to Claim 17, further comprising the following for each cell in said first and second tiles:

a vertical bus extension connected to said configurable terminal switching circuit;

an additional configurable terminal switching circuit connected to said vertical bus extension;

an additional horizontal bus linking said additional configurable terminal switching circuit with said additional configurable terminal switching circuit in a different cell;

an additional switching circuit;

an additional ALU connected to said vertical bus

extension via said additional switching circuit; and

an additional carry propagation bus linking said additional ALU with said additional ALU in the different cell.

19. (New) A configurable electronic circuit according to Claim 18, further comprising an additional bus linking said additional ALU with said ALU in an adjacent cell in a same column.

20. (New) A configurable electronic circuit according Claim 11, further comprising a substrate with said at least one tile formed thereon so that the configurable electronic circuit is an integrated circuit.

21. (New) A configurable electronic circuit comprising:

a plurality of tiles interconnected;

a respective sign extension module connected between adjacent tiles in a row;

each tile comprising a plurality of cells interconnected, each cell comprising

a multiplier,

an arithmetic and logic unit (ALU) for performing at least one arithmetic and/or logic function from a set of functions,

a vertical bus,

a first configurable switching circuit connected to said vertical bus and to inputs of said multiplier,

a second configurable switching circuit connected to said vertical bus and to an output of

said multiplier,

a third configurable switching circuit connected to said vertical bus and to an output of said multiplier in a different cell,

a fourth configurable switching circuit connected to said vertical bus and to inputs of said ALU,

a fifth configurable switching circuit connected to said vertical bus and to an output of said ALU,

a carry propagation bus linking said ALU with said ALU in the different cell,

a configurable terminal switching circuit connected to said vertical bus, and

a horizontal bus linking said configurable terminal switching circuit with said configurable terminal switching circuit in the different cell.

22. (New) A configurable electronic circuit according to Claim 21, wherein said plurality of cells include first and second cells; wherein each multiplier comprises an m*n bit multiplier having two inputs for receiving two words of m and n bits respectively, and the output of each multiplier provides an output word of m+n bits; wherein said second configurable switching circuit in the first cell receives n bits of an output word delivered by said multiplier in the same cell; wherein said third configurable switching circuit of the first cell receives n bits of the output word delivered by said multiplier in the second cell; wherein said second configurable switching circuit in the second cell receives m bits of the output word delivered by said

multiplier in the second cell; and wherein said third configurable switching circuit in the second cell receives m bits of the output word delivered by said multiplier in the first cell.

23. (New) A configurable electronic circuit according to Claim 22, wherein said vertical bus, said carry propagation bus and said horizontal bus each conveys words having a number of bits at least equal to a lowest common multiple of m and of n.

24. (New) A configurable electronic circuit according to Claim 22, wherein m is equal to n, and said vertical bus, said carry propagation bus and said horizontal bus each comprises p tracks of n bits, with p being an integer greater than 1.

25. (New) A configurable electronic circuit according to Claim 21, wherein said plurality of tiles are interconnected in a quincunx form.

26. (New) A configurable electronic circuit according to Claim 21, wherein said plurality of tiles include first and second tiles; each respective sign extension module being connected between said ALU in one cell in said first tile and said vertical bus of an immediately adjacent the cell in said second tile.

27. (New) A configurable electronic circuit according to Claim 26, further comprising the following for each cell in said first and second tiles:

a vertical bus extension connected to said configurable terminal switching circuit;

an additional configurable terminal switching circuit connected to said vertical bus extension;

an additional horizontal bus linking said additional configurable terminal switching circuit with said additional configurable terminal switching circuit in a different cell;

an additional switching circuit;

an additional ALU connected to said vertical bus extension via said additional switching circuit; and

an additional carry propagation bus linking said additional ALU with said additional ALU in the different cell.

28. (New) A configurable electronic circuit according to Claim 27, further comprising an additional bus linking said additional ALU with said ALU in an adjacent cell in a same column.

29. (New) A configurable electronic circuit according Claim 21, further comprising a substrate with said plurality of tiles formed thereon so that the configurable electronic circuit is an integrated circuit.

30. (New) A method for making a configurable electronic circuit comprising:

interconnecting a plurality of cells in at least one tile, the interconnecting for each cell comprising

connecting a first configurable switching circuit to a vertical bus and to inputs of a multiplier,

connecting a second configurable switching

circuit to the vertical bus and to an output of the multiplier,

connecting a third configurable switching circuit to the vertical bus and to an output of a multiplier in a different cell,

connecting a fourth configurable switching circuit to the vertical bus and to inputs of an arithmetic and logic unit (ALU),

connecting a fifth configurable switching circuit to the vertical bus and to an output of the ALU,

connecting a carry propagation bus between the ALU and an ALU in the different cell,

connecting a configurable terminal switching circuit to the vertical bus, and

connecting a horizontal bus between the configurable terminal switching circuit and a configurable terminal switching circuit in the different cell.

31. (New) A method according to Claim 30, wherein the plurality of cells include first and second cells; wherein each multiplier comprises an m*n bit multiplier having two inputs for receiving two words of m and n bits respectively, and the output of each multiplier provides an output word of m+n bits; wherein the second configurable switching circuit in the first cell receives n bits of an output word delivered by the multiplier in the same cell; wherein the third configurable switching circuit of the first cell receives n bits of the output word delivered by the multiplier in the second cell; wherein the second configurable switching circuit

in the second cell receives m bits of the output word delivered by the multiplier in the second cell; and wherein the third configurable switching circuit in the second cell receives m bits of the output word delivered by the multiplier in the first cell.

32. (New) A method according to Claim 31, wherein the vertical bus, the carry propagation bus and the horizontal bus each conveys words having a number of bits at least equal to a lowest common multiple of m and of n.

33. (New) A method according to Claim 31, wherein m is equal to n, and the vertical bus, the carry propagation bus and the horizontal bus each comprises p tracks of n bits, with p being an integer greater than 1.

34. (New) A method according to Claim 30, wherein the at least one tile comprises a plurality of tiles interconnected in a quincunx form.

35. (New) A method according to Claim 34, wherein the plurality of tiles include first and second tiles in a row; further comprising connecting a sign extension module between the first and second tiles, the sign extension module being connected between the ALU in one cell in the first tile and the vertical bus of an immediately adjacent cell in the second tile.

36. (New) A method according to Claim 35, further comprising the following for each cell in the first and second tiles:

connecting a vertical bus extension to the configurable terminal switching circuit;

connecting an additional configurable terminal switching circuit to the vertical bus extension;

connecting an additional horizontal bus between the additional configurable terminal switching circuit and the additional configurable terminal switching circuit in a different cell;

connecting an additional ALU to the vertical bus extension via an additional switching circuit; and

connecting an additional carry propagation bus between the additional ALU and an additional ALU in the different cell.

37. (New) A method according to Claim 36, further comprising connecting an additional bus between the additional ALU and the ALU in an adjacent cell in a same column.